8-Bit Bus Front-Loading Latch Transceivers

SN54/74LS646
SN54/74LS648
SN54/74LS647
SN54/74LS649

Features/Benefits

- Bidirection bus transceivers and registers
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® saves space
- 3-state or open-collector outputs drive bus lines

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	O/P	POWER
SN54LS646	JS,W,L	Mil	Non-invert	3-state	LS
SN74LS646	NS,JS	Com			
SN54LS647	JS,W,L	Mil		Open-collector	
SN74LS647	NS,JS	Com			
SN54LS648	JS,W,L	Mil	Invert	3-state	
SN74LS648	NS,JS	Com			
SN54LS649	JS,W,L	Mil		Open-collector	
SN74LS649	NS,JS	Com			

NOTE: L package here is L28. The other packages are 24-pin.

Description

The 8-bit bus transceivers with 3-state ('LS646, 'LS648) or open-collector ('LS647, 'LS649) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS646/647 and 'LS648/649 are given in their respective Functional Block Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

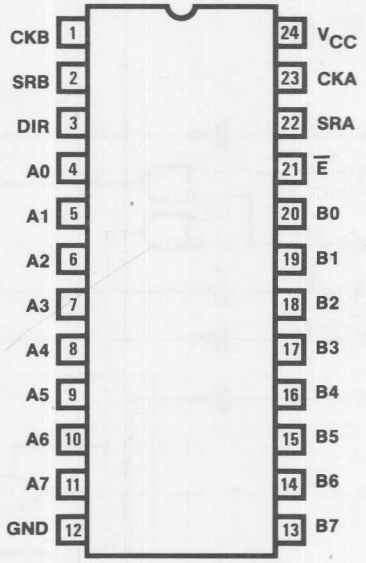
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{E}$, and direction line DIR.

When $\overline{E}$ is High, data from the buses can be stored into register A and B. When $\overline{E}$ is Low and DIR is High, the direction of operation is from A to B; when $\overline{E}$ and DIR are Low, the direction of operation is from B to A.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

Pin Configuration

'LS646/647/648/649
8-Bit Bus Front-Loading
Latch Transceivers



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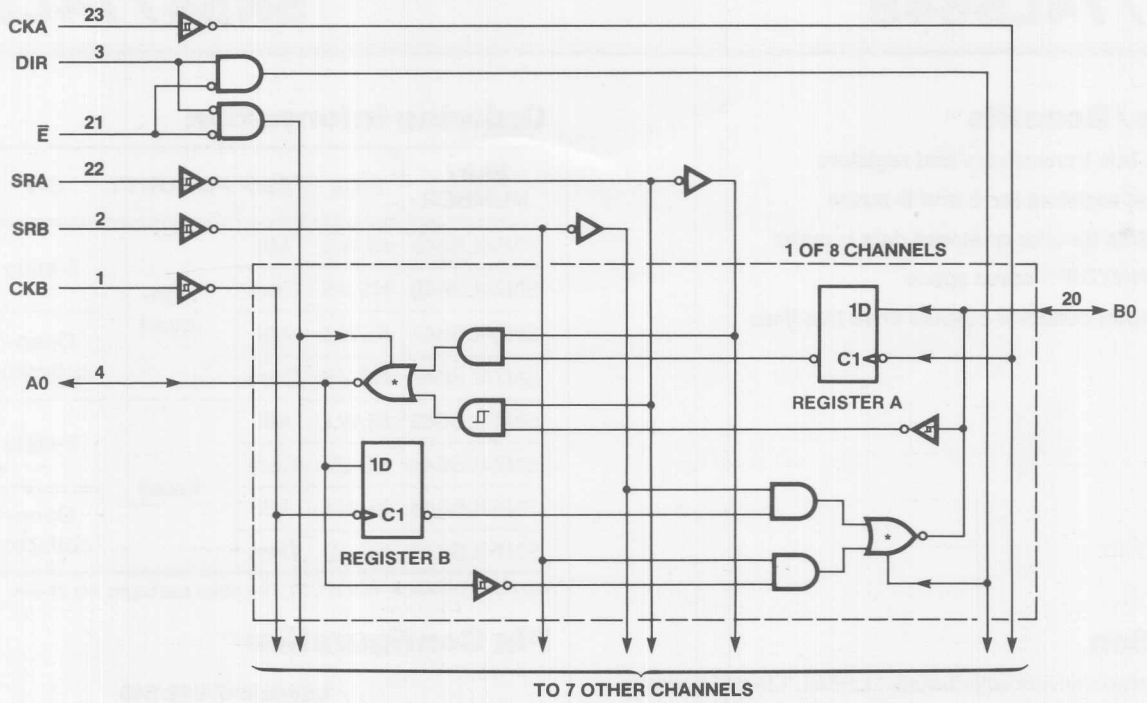
2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories MMI

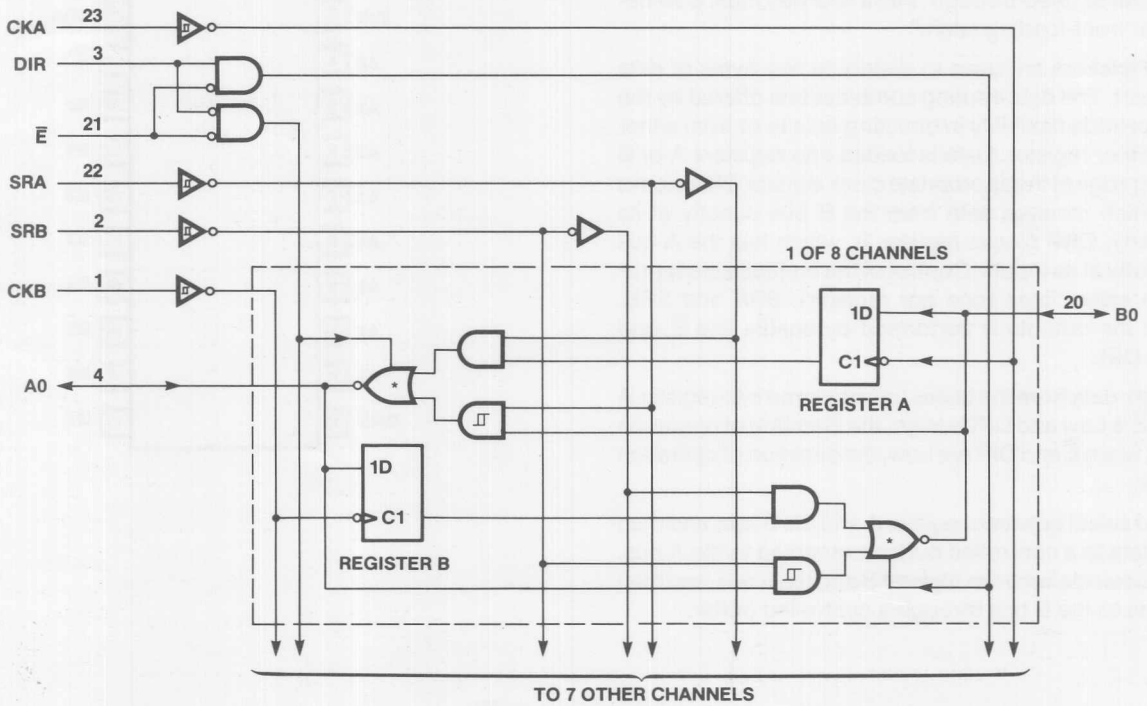
Functional Block Diagrams

'LS646/647 (Non-Inverting)



* For the 'LS646 devices, the A and B bus outputs are 3-state.
For 'LS647 devices, the A and B bus outputs are open-collector.

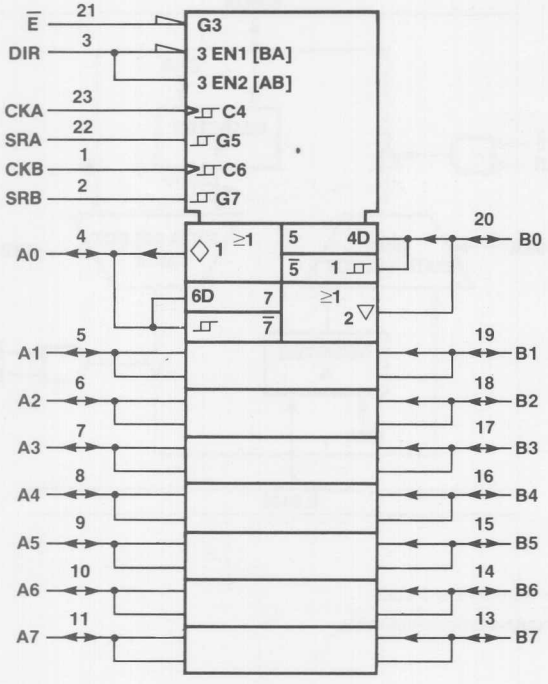
'LS648/649 (Inverting)



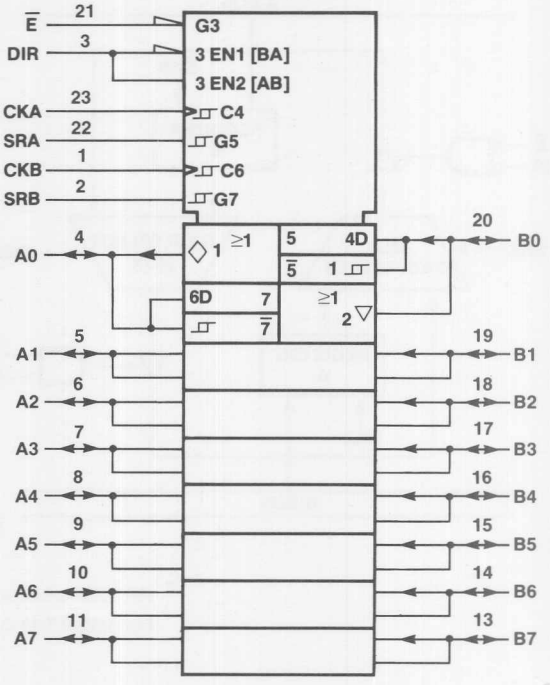
* For the 'LS648 devices, the A and B bus outputs are 3-state.
For 'LS649 devices, the A and B bus outputs are open-collector.

IEEE Symbols

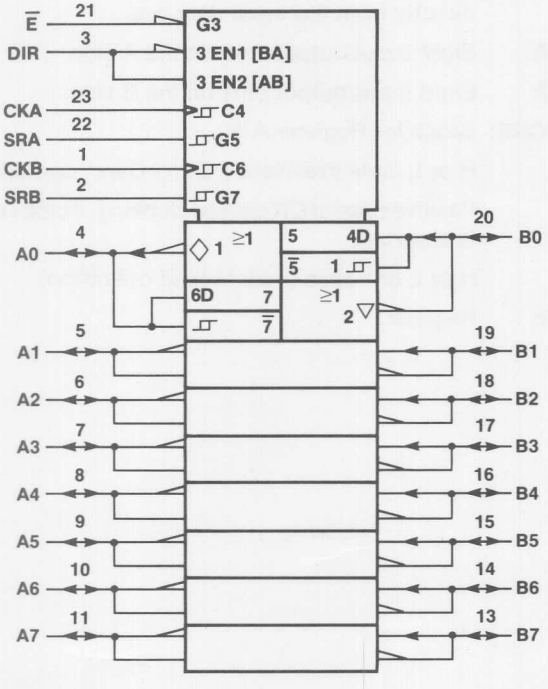
'LS646



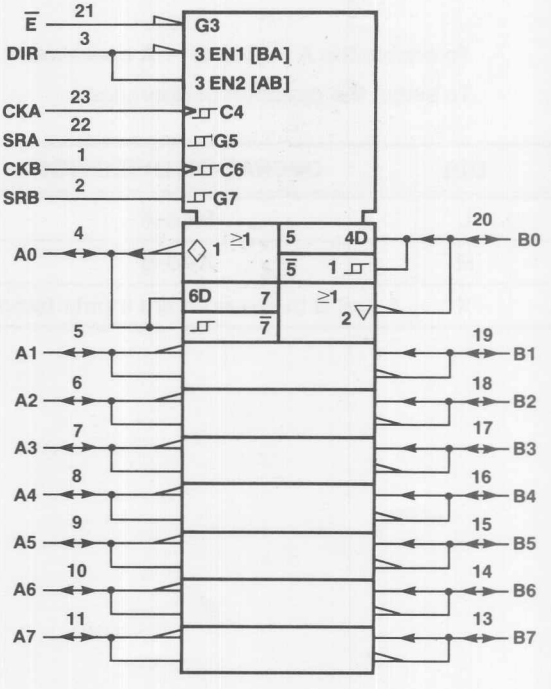
'LS647



'LS648

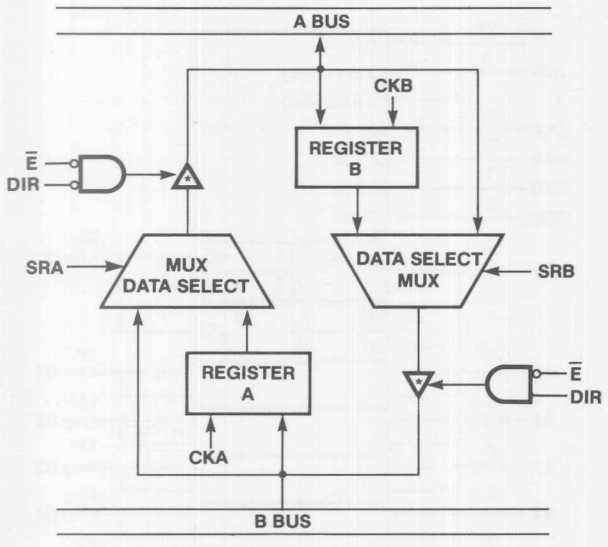


'LS649

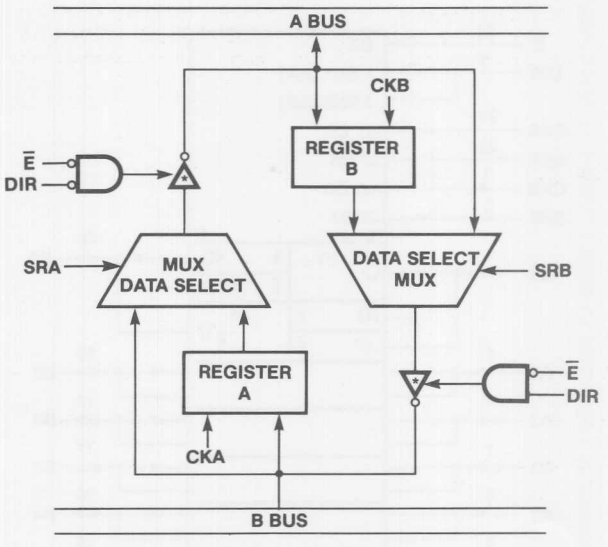


Block Diagrams

'LS646/647 (Non-Inverting)



'LS648/649 (Inverting)



* For 'LS646/648 devices, the A and B bus outputs are 3-state.
For 'LS647/649 devices, the A and B outputs are open-collector.

Function Table Nomenclature Description

$\overline{E}$: To enable the A → B or B → A operation.

DIR: To select the direction of operation.

$\overline{E}$	DIR	OPERATION DIRECTION
L	L	B-to-A
L	H	A-to-B
H	X	A and B buses both are inputs (storage)

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

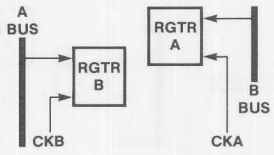
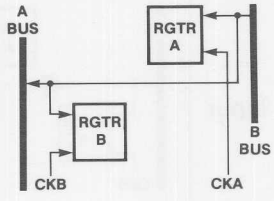
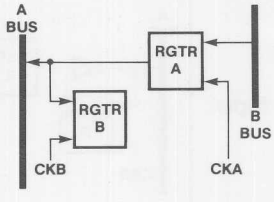
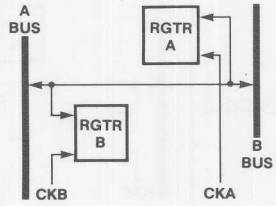
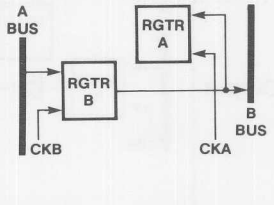
X: H or L state irrelevant ("Don't Care" conditions).

↑: Positive edge of CK causes clocking, if clock enable is asserted.

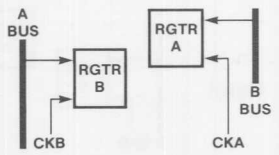
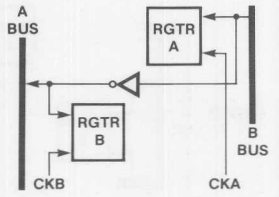
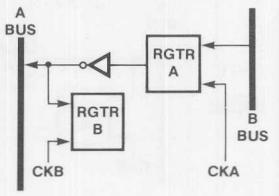
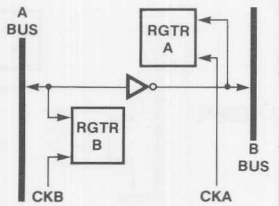
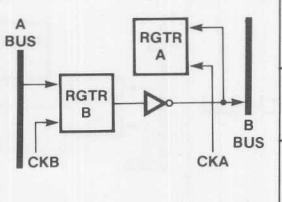
UC: H or L or ↓ case (nonclocked operation).

RGTR: Register.

Bus Management for 'LS646/647

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS646/647
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time B bus data → A bus
								UC	↑	Real time B bus data → A bus Real time B bus data → RGTR B
								↑	UC	Real time B bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR A data → A bus
								UC	↑	RGTR A data → A bus RGTR A data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR A data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time A bus data → B bus
								UC	↑	Real time A bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time A bus data → B bus Real time A bus data → RGTR A
								↑	↑	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR B data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR B data → B bus
								↑	UC	RGTR B data → B bus RGTR B data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

Bus Management for 'LS648/649

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE		'LS648/649
	$\overline{E}$	DIR	SRA	SRB	A0-A7	B0-B7		CKA	CKB	
Storage	H	X	X	X	Input	Input		UC	UC	No operation
								UC	↑	Real time A bus data → RGTR B
								↑	UC	Real time B bus data → RGTR A
								↑	↑	Real time A bus data → RGTR B Real time B bus data → RGTR A
Real time B-to-A Operation	L	L	L	X	Output	Input		UC	UC	Real time $\overline{B}$ bus data → A bus
								UC	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR B
								↑	UC	Real time $\overline{B}$ bus data → A bus Real time B bus data → RGTR A
								↑	↑	Real time $\overline{B}$ bus data → A bus Real time $\overline{B}$ bus data → RGTR A Real time $\overline{B}$ bus data → RGTR B
Stored data B-to-A Operation	L	L	H	X	Output	Input		UC	UC	RGTR $\overline{A}$ data → A bus
								UC	↑	RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
								↑	UC	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus
								↑	↑	Real time B bus data → RGTR A RGTR $\overline{A}$ data → A bus RGTR $\overline{A}$ data → RGTR B
Real time A-to-B Operation	L	H	X	L	Input	Output		UC	UC	Real time $\overline{A}$ bus data → B bus
								UC	↑	Real time $\overline{A}$ bus data → B bus Real time A bus data → RGTR B
								↑	UC	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A
								↑	↑	Real time $\overline{A}$ bus data → B bus Real time $\overline{A}$ bus data → RGTR A Real time A bus data → RGTR B
Stored data A-to-B Operation	L	H	X	H	Input	Output		UC	UC	RGTR $\overline{B}$ data → B bus
								UC	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus
								↑	UC	RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A
								↑	↑	Real time A bus data → RGTR B RGTR $\overline{B}$ data → B bus RGTR $\overline{B}$ data → RGTR A

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... 7.0 V
Input voltage, ... 7.0 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS646	20 ↑			20 ↑			ns
		'LS648	20 ↑			20 ↑			
t_h	Hold time	'LS646	0 ↑			0 ↑			ns
		'LS648	0 ↑			0 ↑			
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2 V	V_O = 0.4 V			−400			−400	μA
I_{OZH}				V_O = 2.7 V			20			20	μA
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	'LS646	V_{CC} = MAX	Outputs High			145			145	mA
				Outputs Low			165			165	
				Outputs Disabled			165			165	
		'LS648		Outputs High			145			145	
				Outputs Low			165			165	
				Outputs Disabled			165			165	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'LS646 MIN	'LS646 MAX	'LS648 MIN	'LS648 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		18		18	ns
t_{PHL}				20		25	ns
t_{PLH}	Clock to output delay			25		25	ns
t_{PHL}				35		40	ns
t_{PLH}	Select to output delay (data input High)			40		55	ns
t_{PHL}				35		40	ns
t_{PLH}	Select to output delay (data input Low)			50		40	ns
t_{PHL}				25		40	ns
t_{PZL}	Output enable delay			65		55	ns
t_{PZH}				55		50	ns
t_{PLZ}	Output disable delay	C_L = 5pF R_L = 667Ω		35		35	ns
t_{PHZ}				35		45	ns
t_{PZL}	Direction enable delay	C_L = 45pF R_L = 667Ω		60		45	ns
t_{PZH}				45		40	ns
t_{PLZ}	Direction disable delay	C_L = 5pF R_L = 667Ω		30		30	ns
t_{PHZ}				30		35	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	MIL 'LS646 MIN	MIL 'LS646 MAX	MIL 'LS648 MIN	MIL 'LS648 MAX	COM 'LS646 MIN	COM 'LS646 MAX	COM 'LS648 MIN	COM 'LS648 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		25		18		25		18	ns
t_{PHL}				25		25		25		25	ns
t_{PLH}	Clock to output delay			28		25		28		25	ns
t_{PHL}				35		40		35		40	ns
t_{PLH}	Select to output delay † (data input High)			40		55		40		55	ns
t_{PHL}				35		40		35		40	ns
t_{PLH}	Select to output delay † (data input Low)			50		40		50		40	ns
t_{PHL}				30		40		30		40	ns
t_{PZL}	Output enable delay			65		55		65		55	ns
t_{PZH}				55		50		55		50	ns
t_{PLZ}	Output disable delay	C_L = 5pF R_L = 667Ω		45		35		45		35	ns
t_{PHZ}				45		50		45		50	ns
t_{PZL}	Direction enable delay	C_L = 45pF R_L = 667Ω		60		45		60		45	ns
t_{PZH}				45		40		45		40	ns
t_{PLZ}	Direction disable delay	C_L = 5pF R_L = 667Ω		40		30		40		30	ns
t_{PHZ}				45		45		45		45	ns

† See Figure 4.

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... 7.0 V
Input voltage, ... 7.0 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature		−55		125	0		75	°C
t_w	Width of clock	High	20			20			ns
		Low	20			20			
t_{su}	Setup time	'LS647	20↑			20↑			ns
		'LS649	20↑			20↑			
t_h	Hold time	'LS647	0↑			0↑			ns
		'LS649	0↑			0↑			
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OL}	Low-level output current				12			24	mA

↑ ↓ The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
ΔV_T	Hysteresis (V_{T+}-V_{T-})		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.4 V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	V_{OH} = 5.5 V			100			100	μA
I_{CC}	Supply current		V_{CC} = MAX	'LS647 Outputs High			130			130	mA
				'LS647 Outputs Low			150			150	
				'LS647 Outputs Disabled			150			150	
				'LS649 Outputs High			130			130	
				'LS649 Outputs Low			150			150	
				'LS649 Outputs Disabled			150			150	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	'LS647 MIN	'LS647 MAX	'LS649 MIN	'LS649 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		26		25	ns
t_{PHL}				27		30	ns
t_{PLH}	Clock to output delay			35		30	ns
t_{PHL}				45		45	ns
t_{PLH}	Select to output delay (data input High)			50		55	ns
t_{PHL}				45		45	ns
t_{PLH}	Select to output delay (data input Low)			60		45	ns
t_{PHL}				30		40	ns
t_{PLH}	Output enable delay			40		40	ns
t_{PHL}				50		50	ns
t_{PLH}	Direction enable delay			35		30	ns
t_{PHL}				40		45	ns

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	MIL 'LS647 MIN	MIL 'LS647 MAX	MIL 'LS649 MIN	MIL 'LS649 MAX	COM 'LS647 MIN	COM 'LS647 MAX	COM 'LS649 MIN	COM 'LS649 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 45pF R_L = 667Ω		32		35		32		35	ns
t_{PHL}				27		30		27		30	ns
t_{PLH}	Clock to output delay			35		40		35		40	ns
t_{PHL}				45		45		45		45	ns
t_{PLH}	Select to output delay (data input High)			50		55		50		55	ns
t_{PHL}				45		45		45		45	ns
t_{PLH}	Select to output delay (data input Low)			60		50		60		50	ns
t_{PHL}				30		40		30		40	ns
t_{PLH}	Output enable delay			40		45		40		45	ns
t_{PHL}				50		50		50		50	ns
t_{PLH}	Direction enable delay			40		45		40		45	ns
t_{PHL}				40		45		40		45	ns

† See Figure 4.

Test Waveform

Setup Time/Hold Time

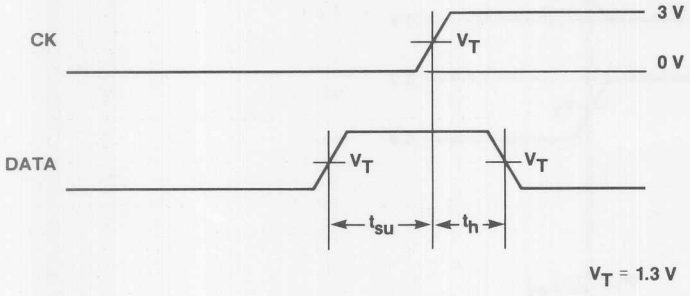


Figure 1.

Bus Data To Bus Output Delay

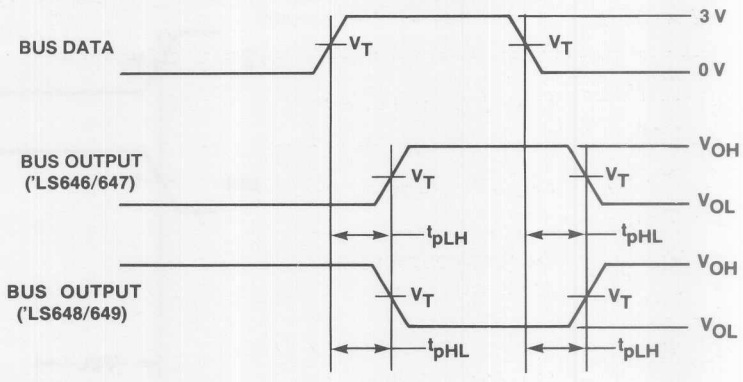


Figure 2.

V_T = 1.3 V

CK To Bus Output Propagation Delay Time

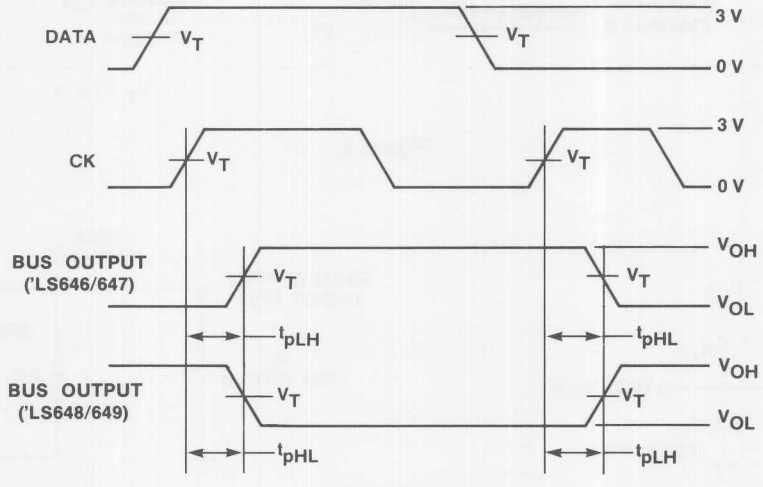


Figure 3.

V_T = 1.3 V

Select To Output Delay

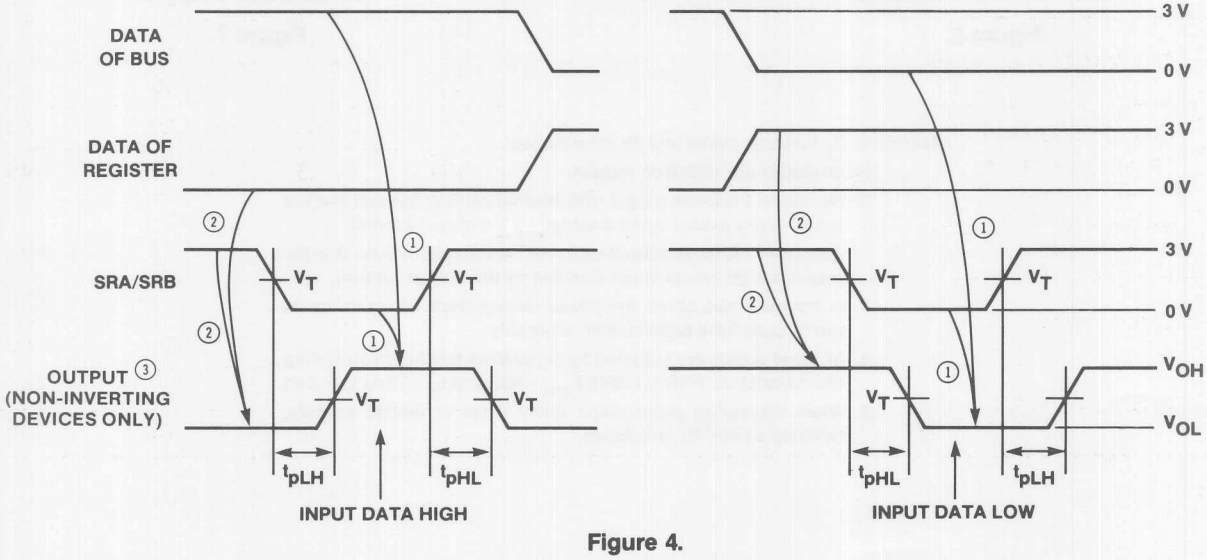


Figure 4.

NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Enable/Disable/Direction-Change Delay

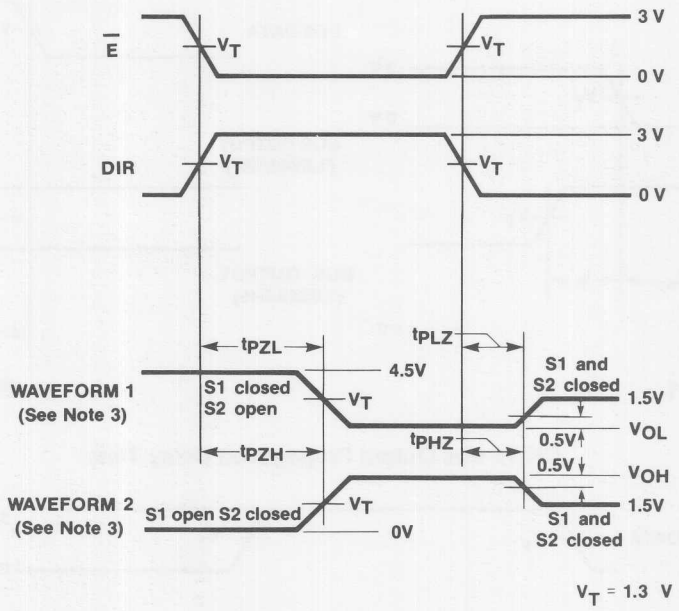
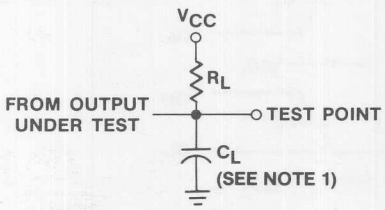


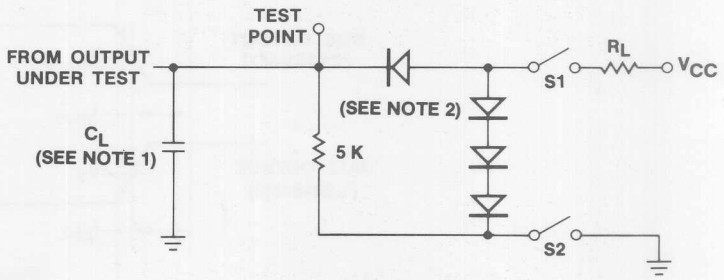
Figure 5.

Test Load



Load Circuit For
Open-Collector Outputs

Figure 6.



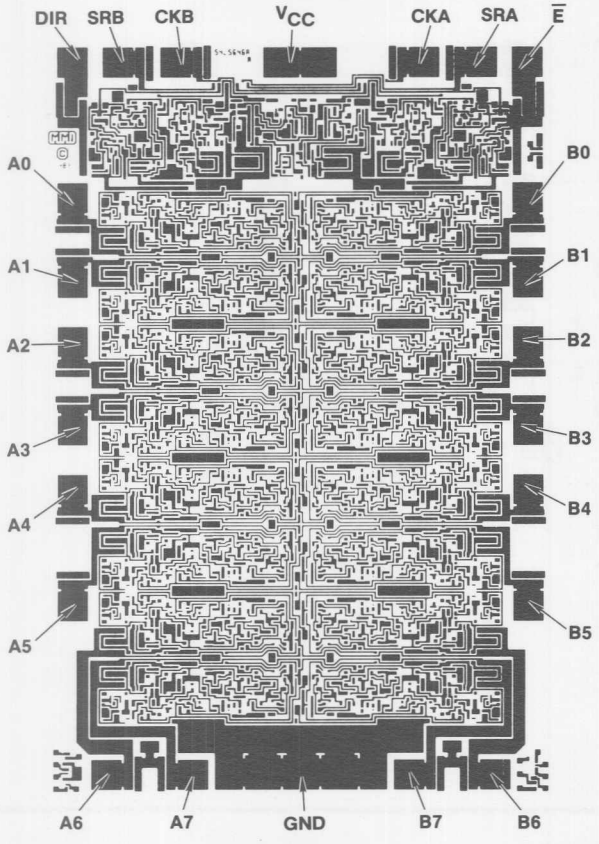
Load Circuit For
Three-State Outputs

Figure 7.

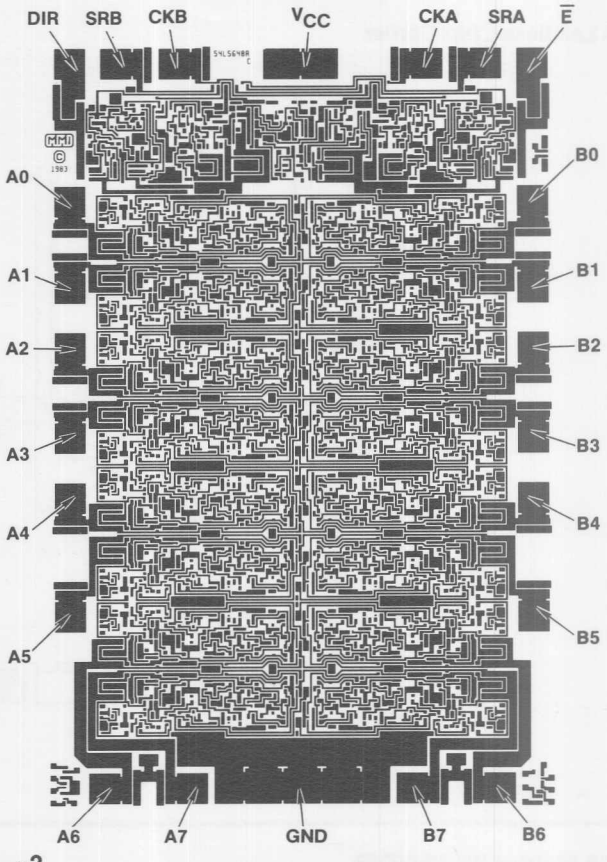
NOTES: 1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.
3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz Z_{out} = 50Ω and t_R = 15 ns t_F ≤ 6 ns
6. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Die Configuration

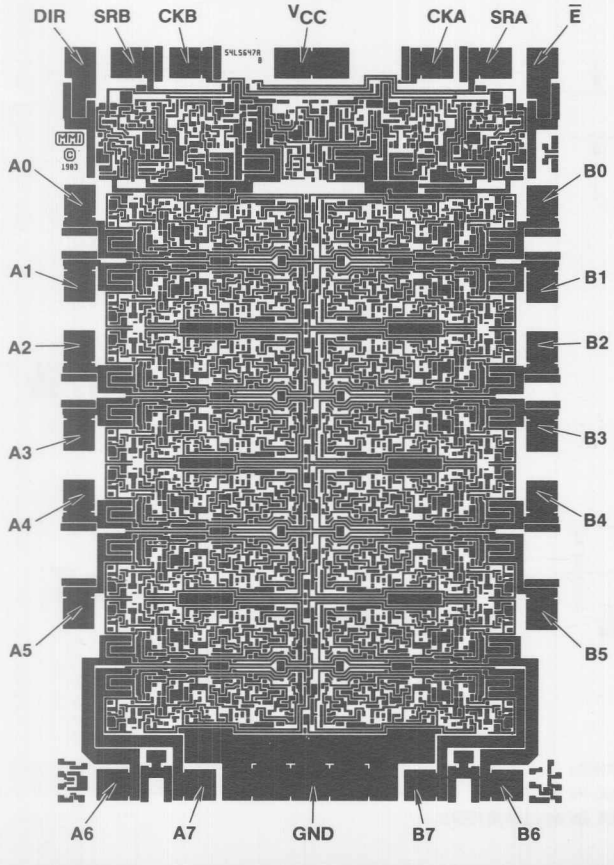
SN54/74LS646



SN54/74LS648

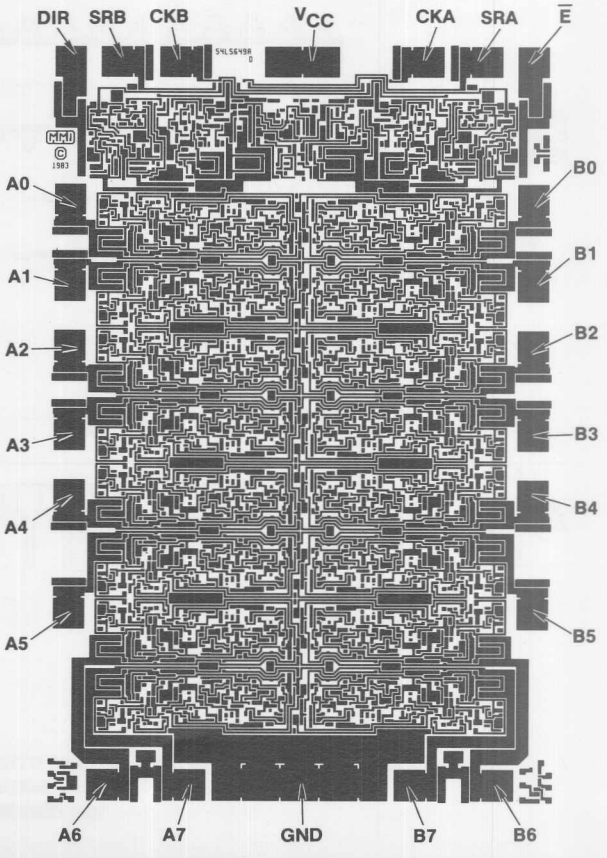


SN54/74LS647



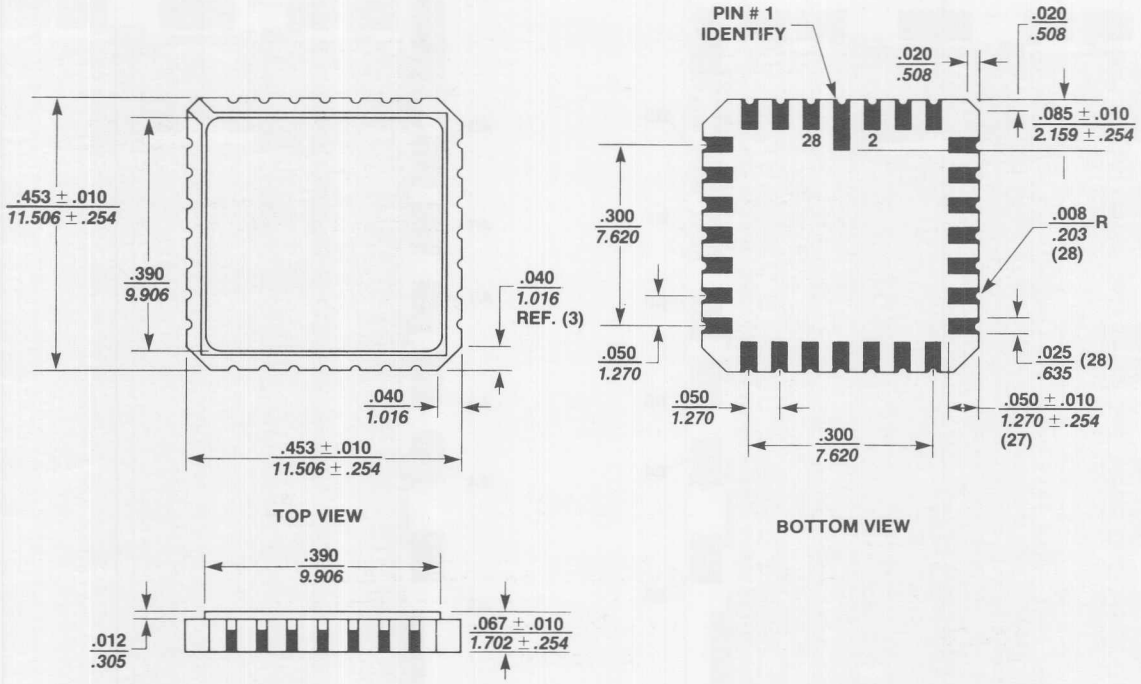
Die size: 93 x 127 mil^2

SN54/74LS649

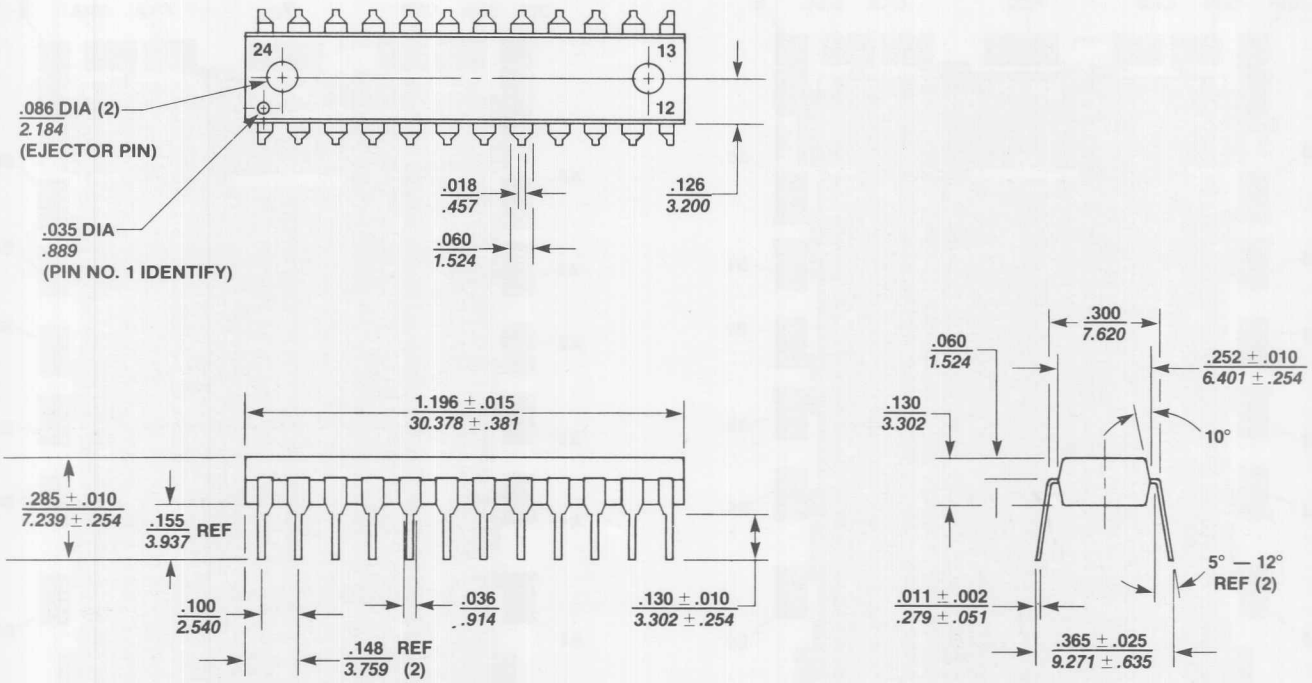


Package Drawings

L28 Leadless Chip Carrier



N24S Molded SKINNYDIP



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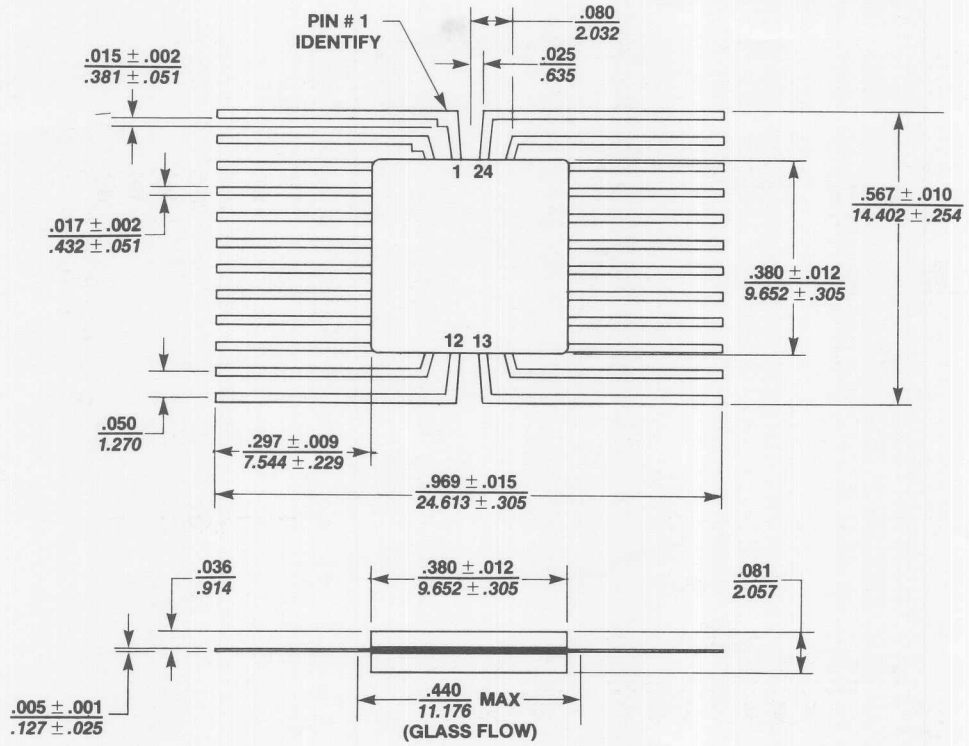
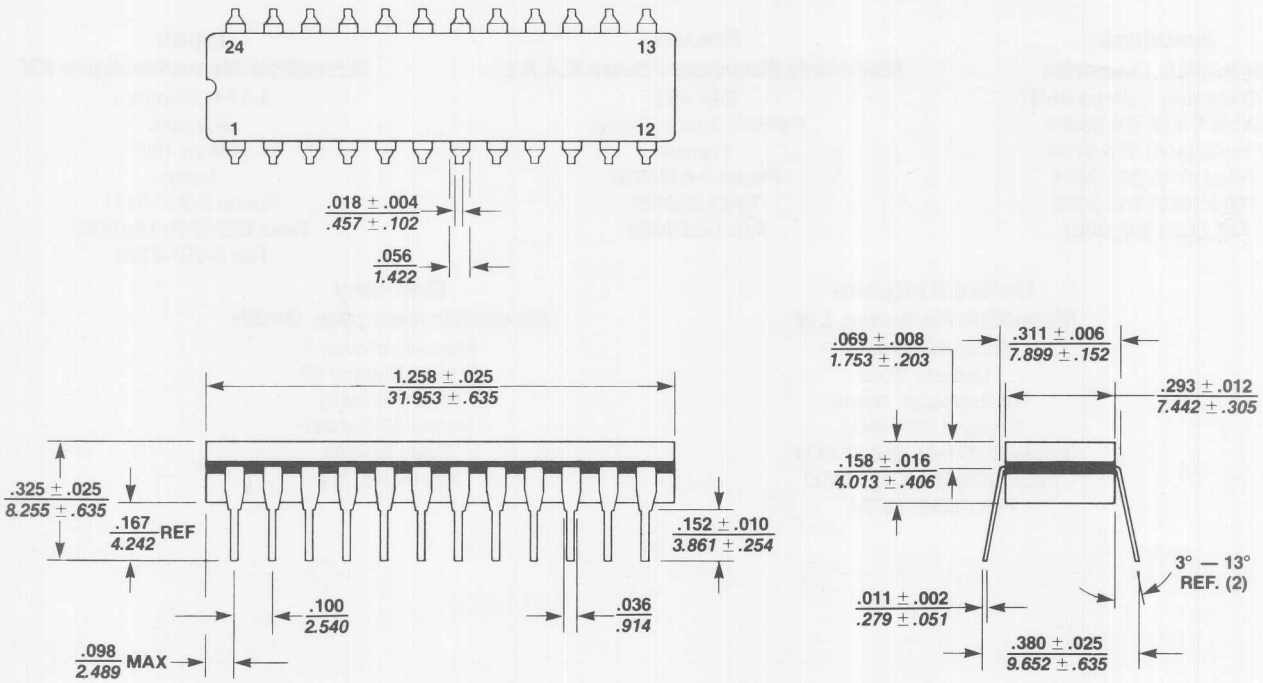
Package Drawings

W24 CERPACK



J24S Ceramic SKINNYDIP



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Monolithic Memories

Americas
Monolithic Memories
2175 Mission College Blvd.
Santa Clara, CA 95050
Phone (408) 970-9700
Telex (910) 338-2374
Telex (910) 338-2376
Fax (408) 988-4254

France
Monolithic Memories France S.A.R.L.
Silic 463
F 94613 Rungis Cedex
France
Phone 1-6874500
Telex 202146
Fax 1-6876825

Japan
Monolithic Memories Japan KK
5-17-9 Shinjuku
Shinjuku
Tokyo 160
Japan
Phone 3-207-3131
Telex 232-3390 MMIKKJ
Fax 3-207-3139

United Kingdom
Monolithic Memories, Ltd.
Monolithic House
1 Queens Road
Farnborough, Hants
England GU146DJ
Phone 9-011-44-252-517431
Telex 858051 MONO UKG
Fax (0252) 43724

Germany
Monolithic Memories, GmbH
Mauerkircherstr 4
D 8000 Munich 80
West Germany
Phone 89-984961
Telex 524385
Fax 89-983162

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